

## **ARIES Embedded Presents New MCXL Reference IP Design**

### **MCXL Embedded Module Relies on Intel Cyclone 10 LP FPGAs and HyperBus Technology for Industrial Control and Communications**

Fuerstenfeldbruck, Germany, March 30, 2022 – ARIES Embedded, a specialist in embedded services and products, enhances the well-proven MCXL System-on-Module (SoM) with the new reference IP design. The MCXL SoM is based on the Intel Cyclone 10 LP family. It is the first FPGA SoM featuring HyperBus Technology. “The new reference design provides an excellent benefit for all customers to evaluate the MCXL SoM or start their own developments,” stated Andreas Widder, Managing Director of ARIES Embedded. “The design implements the VexRiscv (open source RISC-V soft-core) running FreeRTOS, as well as Intel Triple Speed Ethernet MAC and the SLL MBMC IP.” The MCXL SoM leverages the functionality of the Cyclone 10 LP family on a compact embedded module. Intel Cyclone 10 LP FPGAs are ideal for cost-sensitive applications that require increasing lower static power as the need for scalable processing acceleration increases system interface requirements. The large range of industrial applications involves I/O expansion, interfacing, bridging, sensor fusion, and industrial motor control.

### **Easy and Fast Project Launch**

For the MCXL reference IP design, three Quartus projects are available: one for the MCXL-S (SDRAM variant) and two for the MCXL-H (HyperBus variant). All implement a RISC-V core with FreeRTOS, a UART core, and GPIO routed to the PMod connectors and gigabit Ethernet using the Intel TSE MAC. The `mcxl_h_ethernet` and `mcxl_s_ethernet` projects use only 128 KiB on-chip memory to provide RAM for the RISC-V core. The `mcxl_h_ethernet_hyperbus` project also implements the SLL HyperBus IP Core, available with a time-limited 30 minutes free trial license providing additional 32 MiB of HyperRAM and 128 MiB of HyperFlash.

Words: 289

**Technical details:**

MCXL Reference IP Design: <https://github.com/ARIES-Embedded/mcxl-reference-designs>

MCXL SoM: <https://www.aries-embedded.com/system-on-module/fpga/cyclone-10lp-intel-fpga-mcxl-som-low-power-cost-sensitive>

Keywords: Aries Embedded, embedded system, FPGA, MCXL, System-on-Module, industrial, industrial communication, bridging, motor control, sensor fusion, Intel, Cyclone 10 LP, Hyperbus

**Images**

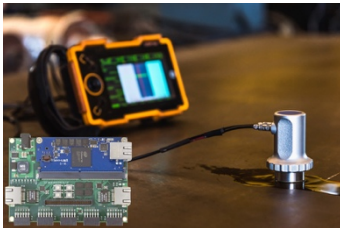


Image 1: New MCXL Reference IP Design for MCXL from ARIES Embedded for Industrial

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Image 2: Andreas Widder is Managing Director of ARIES Embedded GmbH

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